WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a ferroelectric capacitor for storing any one of a plurality of logic values such that a plurality of different displacements of a remanent polarization correspond to at least one of said plurality of logic values, while another displacement of the remanent polarization different from each of the plurality of displacements of the remanent polarization corresponds to each of the plurality of logic values other than the at least one logic value;

data writing means for applying, to the ferroelectric capacitor, at least one write electric voltage pulse for poling the ferroelectric capacitor in any one of the plurality of displacements and the other displacement and thereby writing any one of the plurality of logic values in the ferroelectric capacitor; and

data reading means for applying a read electric voltage pulse to the ferroelectric capacitor, sensing the displacement of the remanent polarization in the ferroelectric capacitor when the read electric voltage pulse is applied, and thereby reading the logic value stored in the ferroelectric capacitor.

2. The semiconductor memory device of claim 1, wherein the write electric voltage pulse for poling the ferroelectric capacitor in any of the plurality of displacements include a plurality of write electric voltage pulses different from each other in potential.

3. The semiconductor memory device of claim 1, wherein the write electric voltage pulses for poling the ferroelectric capacitor into any of the plurality of displacements include a plurality of write electric voltage pulses different from each other in pulse width.

4. The semiconductor memory device of claim 1, wherein, when the other displacement of the remanent polarization includes only one other displacement, the displacement is zero or in the vicinity of zero and, when the other displacement of the

remanent polarization includes a plurality of other displacements, one of the plurality of displacements is zero or in the vicinity of zero.

5. The semiconductor memory device of claim 1, wherein the read electric voltage pulse has been set to a value such that, when the read electric voltage pulse is removed, the displacement of the remanent polarization in the ferroelectric capacitor is restored to the original displacement before the application of the read electric voltage pulse.

6. The semiconductor memory device of claim 1, further comprising:

a capacitance load connected in series to the ferroelectric capacitor, wherein

the data reading means has means for applying the read electric voltage pulse to both ends of a series circuit composed of the ferroelectric capacitor and the capacitance load and

the capacitance load has been set to a value such that, when the read electric voltage pulse is removed, the displacement of the remanent polarization in the ferroelectric capacitor is restored to the displacement prior to the application of the read electric voltage pulse.

7. The semiconductor memory device of claim 1, wherein the data writing means applies, during a normal operation, the write electric voltage pulse for poling the ferroelectric capacitor into the one of the plurality of displacements having a relatively small absolute value, while applying, in each specified cycle or immediately before a transition to a specified operating condition, the write electric voltage pulse for poling the ferroelectric capacitor into the one of the plurality of displacements having a relatively large absolute value.

8. The semiconductor memory device of claim 7, further comprising:

a clock counter for counting clock pulses inputted from the outside or internally generated clock pulses; and

control means for causing, based on a signal from the clock counter, the data writing means to apply the write electric voltage pulse for poling the ferroelectric capacitor in the one of the plurality of displacements having a relatively large absolute value in each specified cycle or immediately before a transition to a specified operating condition.

9. An electronic apparatus, comprising:

the semiconductor memory device as recited in claim 7; and

a system control device for monitoring an operating state of a system and causing the data writing means to apply the write electric voltage pulse for poling the ferroelectric capacitor into the one of the plurality of displacements having a relatively large absolute value in each specified cycle or immediately before a transition to a specified operating condition.

10. An electronic apparatus, comprising:

the semiconductor memory device as recited in claim 7; and

a system control device for monitoring a power source for driving a system and causing the data writing means to apply the write electric voltage pulse for poling the ferroelectric capacitor into the one of the plurality of displacements having a relatively large absolute value immediately before a power supply from the power source is halted or immediately before the power source shifts to a power saving condition.

11. The electronic apparatus of claim 10, wherein the power source is a primary battery or a secondary battery.